

What is claimed is:

1 1. A nonvolatile memory microcomputer chip comprising a  
2 microcomputer unit and a memory unit,  
3 the microcomputer unit including:  
4 a plurality of circuit blocks including a CPU, and  
5 the memory unit including:  
6 a nonvolatile memory;  
7 a memory control unit operable to (a) acquire a  
8 plurality of pieces of test data from outside the  
9 nonvolatile memory microcomputer chip and store the  
10 plurality of pieces of test data in the nonvolatile memory,  
11 and then (b) control the nonvolatile memory to sequentially  
12 output a plurality of test signals which each show a piece  
13 of test data out of the plurality of pieces of test data;  
14 a drive unit operable to supply each of the plurality  
15 of test signals sequentially output from the nonvolatile  
16 memory, to any of the plurality of circuit blocks that  
17 is to be tested using a piece of test data shown by the  
18 test signal, to drive the circuit block; and  
19 an output unit operable to receive a test result signal  
20 from the driven circuit block, and output the test result  
21 signal to outside the nonvolatile memory microcomputer  
22 chip.

1 2. The nonvolatile memory microcomputer chip of Claim 1,

2            wherein the microcomputer unit further includes:  
3            a port operable to send/receive a signal to/from  
4 outside the microcomputer unit,  
5            the drive unit supplies the test signal to the circuit  
6 block through the port, and  
7            the output unit receives the test result signal from  
8 the circuit block through the port.

1    3. The nonvolatile memory microcomputer chip of Claim 2,  
2            wherein the memory control unit (a) acquires a  
3 plurality of pieces of expectation data from outside the  
4 nonvolatile memory microcomputer chip in a one-to-one  
5 correspondence with the plurality of pieces of test data,  
6 and stores each piece of test data and a corresponding  
7 piece of expectation data in a memory area of the nonvolatile  
8 memory having a unique address, each piece of expectation  
9 data representing a test result signal that is expected  
10 if a circuit block to which a test signal showing a  
11 corresponding piece of test data is output is driven  
12 correctly, and then (b) each time an address signal is  
13 given from outside the nonvolatile memory microcomputer  
14 chip, controls the nonvolatile memory to output a test  
15 signal and an expectation signal that respectively show  
16 a piece of test data and a piece of expectation data stored  
17 in a memory area having an address shown by the address

18 signal,  
19 the drive unit supplies the test signal output from  
20 the nonvolatile memory in response to the address signal,  
21 to a circuit block that is to be tested using the piece  
22 of test data shown by the test signal, to drive the circuit  
23 block, and  
24 the output unit receives a test result signal from  
25 the driven circuit block, and outputs the test result signal  
26 and the expectation signal together to outside the  
27 nonvolatile memory microcomputer chip.

1 4. The nonvolatile memory microcomputer chip of Claim 1,  
2 further comprising:

3 an address generation unit operable to sequentially  
4 output a plurality of address signals,

5 the memory control unit (a) stores each piece of test  
6 data in a memory area of the nonvolatile memory having  
7 a unique address, and then (b) each time the address  
8 generation unit outputs an address signal, controls the  
9 nonvolatile memory to output a test signal showing a piece  
10 of test data stored in a memory area having an address  
11 shown by the address signal, and

12 the drive unit supplies the test signal output from  
13 the nonvolatile memory in response to the address signal,  
14 to a circuit block that is to be tested using the piece

15 of test data shown by the test signal, to drive the circuit  
16 block.

1 5. The nonvolatile memory microcomputer chip of Claim 4,  
2 wherein the memory control unit (a) acquires a  
3 plurality of pieces of control data from outside the  
4 nonvolatile memory microcomputer chip in a one-to-one  
5 correspondence with the plurality of pieces of test data,  
6 and stores each piece of control data in a memory area  
7 of the nonvolatile memory in which a corresponding piece  
8 of test data is stored, the plurality of pieces of control  
9 data designating an order in which the plurality of pieces  
10 of test data are used, and then (b) each time the address  
11 generation unit outputs an address signal, controls the  
12 nonvolatile memory to output a test signal and a control  
13 signal which respectively show a piece of test data and  
14 a piece of control data stored in a memory area having  
15 an address shown by the address signal, and

16 the address generation unit includes:

17 a counter unit holding a count value, and operable  
18 to periodically output an address signal showing the count  
19 value and increment the count value by 1; and

20 a counter control unit operable to (i) store the count  
21 value held by the counter unit when the nonvolatile memory  
22 outputs a control signal showing a piece of control data

23 having a first value, and subsequently (ii) replaces the  
24 count value held by the counter unit with the stored count  
25 value when the nonvolatile memory outputs a control signal  
26 showing a piece of control data having a second value.

1 6. The nonvolatile memory microcomputer chip of Claim 4,  
2 wherein the plurality of pieces of test data are  
3 divided into test data groups, with a piece of test data  
4 at the end of each test data group being end data that  
5 can be distinguished from other pieces of test data, and  
6 the address generation unit includes:  
7 an address storage unit operable to store an address  
8 of a memory area of the nonvolatile memory in which a piece  
9 of test data at the beginning of each test data group is  
10 stored;  
11 a counter unit holding a count value, and operable  
12 to periodically output an address signal showing the count  
13 value and increment the count value by 1; and  
14 a counter control unit operable to replace the count  
15 value held by the counter unit with one of addresses stored  
16 in the address storage unit, when the nonvolatile memory  
17 outputs a test signal showing the end data.

1 7. The nonvolatile memory microcomputer chip of Claim 4,  
2 wherein the plurality of pieces of test data are

3 divided into test data groups, with a piece of test data  
4 at the end of each test data group being end data that  
5 can be distinguished from other pieces of test data,  
6 the address generation unit includes:  
7 an address storage unit operable to acquire a  
8 plurality of addresses and a plurality of control flag  
9 values which are in a one-to-one correspondence with each  
10 other from outside the nonvolatile memory microcomputer  
11 chip, and store the plurality of addresses and the plurality  
12 of control flag values beforehand; and  
13 a release signal acquisition unit operable to acquire  
14 a release signal from outside the nonvolatile memory  
15 microcomputer chip, and  
16 the address generation unit, for each address stored  
17 in the address storage unit,  
18 (1) outputs an address signal showing the address,  
19 (2) if a corresponding control flag value is a first  
20 value, subsequently outputs address signals which show  
21 consecutive addresses following the address in sequence,  
22 until the nonvolatile memory outputs a test signal showing  
23 the end data, and  
24 (3) if the corresponding control flag value is a second  
25 value, subsequently outputs address signals which  
26 uniformly show the address in sequence, until the release  
27 signal acquisition unit acquires the release signal.

1 8. The nonvolatile memory microcomputer chip of Claim 1,  
2 wherein the memory control unit includes:  
3 an address adjustment unit operable to:  
4 (1) hold a repetition start address, a repetition  
5 end address, and a repetition number;  
6 (2) sequentially receive a plurality of address  
7 signals; and  
8 (3) each time an address signal is received, (i) output  
9 the address signal if an address shown by the address signal  
10 is different from the repetition start address, and (ii)  
11 repeat, a number of times equivalent to the repetition  
12 number, outputting address signals which show consecutive  
13 addresses from the repetition start address to the  
14 repetition end address in sequence, if the address shown  
15 by the address signal is same as the repetition start  
16 address,  
17 the memory control unit (a) stores each piece of test  
18 data in a memory area of the nonvolatile memory having  
19 a unique address, and then (b) each time the address  
20 adjustment unit outputs an address signal, controls the  
21 nonvolatile memory to output a test signal showing a piece  
22 of test data stored in a memory area having an address  
23 shown by the address signal, and  
24 the drive unit supplies the test signal output from

25 the nonvolatile memory in response to the address signal,  
26 to a circuit block that is to be tested using the piece  
27 of test data shown by the test signal, to drive the circuit  
28 block.

1 9. The nonvolatile memory microcomputer chip of Claim 3,  
2 wherein at least two pieces of test data out of the  
3 plurality of pieces of test data have different bit lengths  
4 according to different contents of the at least two pieces  
5 of test data,

6 the drive unit supplies a mixed signal to the port,  
7 the mixed signal being made up of a test signal showing  
8 a piece of test data whose bit length is not largest among  
9 the plurality of pieces of test data and one part of an  
10 expectation signal output from the nonvolatile memory  
11 together with the test signal, and

12 the port extracts the test signal from the mixed signal  
13 according to contents of the mixed signal, and supplies  
14 the extracted test signal to a circuit block that is to  
15 be tested using the piece of test data shown by the test  
16 signal.

1 10. The nonvolatile memory microcomputer chip of Claim  
2 1,

3 wherein the drive unit shifts the test signal in level



4 based on an input signal reference voltage applied from  
5 outside the nonvolatile memory microcomputer chip, and  
6 supplies the shifted test signal to the circuit block to  
7 drive the circuit block, and  
8 the output unit shifts the test result signal in level  
9 based on a comparison reference voltage applied from  
10 outside the nonvolatile memory microcomputer chip, and  
11 outputs the shifted test result signal to outside the  
12 nonvolatile memory microcomputer chip.

1 11. The nonvolatile memory microcomputer chip of Claim  
2 1, further comprising:

3 a plurality of pairs of connection lines which are  
4 provided in a one-to-one correspondence with the plurality  
5 of circuit blocks, and each operable to transfer a signal  
6 between a corresponding circuit block and the drive unit  
7 and between the corresponding circuit block and the output  
8 unit,

9 the drive unit supplies the test signal to the circuit  
10 block through one connection line out of a pair of connection  
11 lines corresponding to the circuit block, and

12 the output unit receives the test result signal from  
13 the circuit block through the other connection line out  
14 of the pair of connection lines corresponding to the circuit  
15 block.

1 12. The nonvolatile memory microcomputer chip of Claim  
2 11,  
3 wherein the memory control unit (a) stores each piece  
4 of test data in a memory area of the nonvolatile memory  
5 having a unique address, and then (b) each time an address  
6 signal is given from outside the nonvolatile memory  
7 microcomputer chip, controls the nonvolatile memory to  
8 output a test signal showing a piece of test data stored  
9 in a memory area having an address shown by the address  
10 signal,  
11 the memory unit further includes:  
12 a circuit block specification unit operable to  
13 specify a circuit block that is to be tested using the  
14 piece of test data shown by the test signal output from  
15 the nonvolatile memory in response to the address signal,  
16 based on the address signal, and  
17 the drive unit supplies the test signal to the circuit  
18 block specified by the circuit block specification unit,  
19 to drive the circuit block.

1 13. The nonvolatile memory microcomputer chip of Claim  
2 11,  
3 wherein the memory control unit (a) acquires a  
4 plurality of pieces of selection data from outside the

5 nonvolatile memory microcomputer chip in a one-to-one  
6 correspondence with the plurality of pieces of test data,  
7 and stores each piece of test data and a corresponding  
8 piece of selection data in a memory area of the nonvolatile  
9 memory having a unique address, each piece of selection  
10 data being used for specifying a circuit block that is  
11 to be tested using a corresponding piece of test data,  
12 and then (b) each time an address signal is given from  
13 outside the nonvolatile memory microcomputer chip,  
14 controls the nonvolatile memory to output a test signal  
15 and a selection signal which respectively show a piece  
16 of test data and a piece of selection data stored in a  
17 memory area having an address shown by the address signal,  
18 and

19 the drive unit supplies the test signal output from  
20 the nonvolatile memory in response to the address signal,  
21 to a circuit block that is specified according to the  
22 selection signal, to drive the circuit block.

1 14. The nonvolatile memory microcomputer chip of Claim  
2 1,

3 wherein the memory unit includes a plurality of  
4 nonvolatile memories,

5 the memory control unit (a) stores the plurality of  
6 pieces of test data in the plurality of nonvolatile memories,

7 and then (b) controls each nonvolatile memory to  
8 sequentially output a plurality of test signals which each  
9 show a piece of test data out of pieces of test data stored  
10 in the nonvolatile memory, in parallel,  
11 wherein if two nonvolatile memories out of the  
12 plurality of nonvolatile memories are to output test  
13 signals showing pieces of test data used for testing a  
14 same circuit block, the memory control unit allows one  
15 of the two nonvolatile memories to output a test signal  
16 and prohibits the other nonvolatile memory from outputting  
17 a test signal, and  
18 the drive unit supplies a test signal output from  
19 each nonvolatile memory, to a circuit block that is to  
20 be tested using a piece of test data shown by the test  
21 signal, to drive the circuit block.

1 15. The nonvolatile memory microcomputer chip of Claim  
2 1,

3 wherein the nonvolatile memory includes:

4 an oscillation circuit operable to generate a first  
5 clock signal, and

6 the nonvolatile memory microcomputer chip further  
7 comprises:

8 a selection circuit operable to selectively supply  
9 one of the first clock signal and a second clock signal

10 which is fed from outside the nonvolatile memory  
11 microcomputer chip, to each circuit block in the  
12 microcomputer unit.

1 16. The nonvolatile memory microcomputer chip of Claim  
2 15,

3 wherein the memory control unit (a) acquires a  
4 plurality of pieces of selection data from outside the  
5 nonvolatile memory microcomputer chip in a one-to-one  
6 correspondence with the plurality of pieces of test data,  
7 and stores each piece of test data and a corresponding  
8 piece of selection data in a memory area of the nonvolatile  
9 memory having a unique address, each piece of selection  
10 data being used for selecting one of the first clock signal  
11 and the second clock signal, and then (b) each time an  
12 address signal is given from outside the nonvolatile memory  
13 microcomputer chip, controls the nonvolatile memory to  
14 output a test signal and a selection signal which  
15 respectively show a piece of test data and a piece of  
16 selection data stored in a memory area having an address  
17 shown by the address signal, and

18 the selection circuit supplies one of the first clock  
19 signal and the second clock signal that is selected  
20 according to the selection signal, to each circuit block  
21 in the microcomputer unit.

1 17. The nonvolatile memory microcomputer chip of Claim  
2 15,

3        wherein the memory control unit (a) acquires a  
4 plurality of pieces of selection data from outside the  
5 nonvolatile memory microcomputer chip in a one-to-one  
6 correspondence with the plurality of pieces of test data,  
7 and stores each piece of test data and a corresponding  
8 piece of selection data in a memory area of the nonvolatile  
9 memory having a unique address, each piece of selection  
10 data being used for selecting a frequency of the first  
11 clock signal, and then (b) each time an address signal  
12 is given from outside the nonvolatile memory microcomputer  
13 chip, controls the nonvolatile memory to output a test  
14 signal and a selection signal which respectively show a  
15 piece of test data and a piece of selection data stored  
16 in a memory area having an address shown by the address  
17 signal, and

18        the oscillation circuit generates the first clock  
19 signal having a frequency that is selected from a plurality  
20 of predetermined frequencies according to the selection  
21 signal.

1 18. The nonvolatile memory microcomputer chip of Claim  
2 1,

3            wherein the memory control unit (a) acquires a  
4   plurality of pieces of selection data from outside the  
5   nonvolatile memory microcomputer chip in a one-to-one  
6   correspondence with the plurality of pieces of test data,  
7   and stores each piece of test data and a corresponding  
8   piece of selection data in a memory area of the nonvolatile  
9   memory having a unique address, each piece of selection  
10   data being used for selecting a delay time, and then (b)  
11   each time an address signal is given from outside the  
12   nonvolatile memory microcomputer chip, controls the  
13   nonvolatile memory to output a test signal and a selection  
14   signal which respectively show a piece of test data and  
15   a piece of selection data stored in a memory area having  
16   an address shown by the address signal,

17           the output unit includes:

18           a delay unit operable to delay a test result signal  
19   received from a circuit block which is driven by the test  
20   signal output from the nonvolatile memory in response to  
21   the address signal, by a delay time that is selected from  
22   a plurality of predetermined delay times according to the  
23   selection signal, and

24           the output unit outputs the delayed test result signal  
25   to outside the nonvolatile memory microcomputer chip.

1   19. The nonvolatile memory microcomputer chip of Claim

2 1,

3 wherein the memory control unit (a) acquires a

4 plurality of pieces of selection data from outside the

5 nonvolatile memory microcomputer chip in a one-to-one

6 correspondence with the plurality of pieces of test data,

7 and stores each piece of test data and a corresponding

8 piece of selection data in a memory area of the nonvolatile

9 memory having a unique address, each piece of selection

10 data being used for selecting a delay time, and then (b)

11 each time an address signal is given from outside the

12 nonvolatile memory microcomputer chip, controls the

13 nonvolatile memory to output a test signal and a selection

14 signal which respectively show a piece of test data and

15 a piece of selection data stored in a memory area having

16 an address shown by the address signal,

17 the drive unit includes:

18 a delay unit operable to delay the test signal output

19 from the nonvolatile memory in response to the address

20 signal, by a delay time that is selected from a plurality

21 of predetermined delay times according to the selection

22 signal, and

23 the drive unit supplies the delayed test signal to

24 a circuit block that is to be tested using the piece of

25 test data shown by the delayed test signal, to drive the

26 circuit block.



1 20. The nonvolatile memory microcomputer chip of Claim  
2 1,  
3 wherein the memory control unit (a) acquires a  
4 plurality of pieces of designation data from outside the  
5 nonvolatile memory microcomputer chip in a one-to-one  
6 correspondence with the plurality of pieces of test data,  
7 and stores each piece of test data and a corresponding  
8 piece of designation data in a memory area of the nonvolatile  
9 memory having a unique address, each piece of designation  
10 data being used for designating a voltage, and then (b)  
11 each time an address signal is given from outside the  
12 nonvolatile memory microcomputer chip, controls the  
13 nonvolatile memory to output a test signal and a designation  
14 signal which respectively show a piece of test data and  
15 a piece of designation data stored in a memory area having  
16 an address shown by the address signal, and  
17 the nonvolatile memory microcomputer chip further  
18 comprises:  
19 a power supply unit operable to adjust a voltage of  
20 external power applied from outside the nonvolatile memory  
21 microcomputer chip to a voltage that is designated  
22 according to the designation signal to generate internal  
23 power, and supply the internal power to a circuit block

24 that is to be tested using the piece of test data shown  
25 by the test signal as operating power.

1 21. The nonvolatile memory microcomputer chip of Claim  
2 20,

3 wherein the plurality of circuit blocks in the  
4 microcomputer unit include:

5 a D/A conversion circuit which serves as the power  
6 supply unit,

7 wherein the D/A conversion circuit generates the  
8 internal power by digital-to-analog converting the piece  
9 of designation data shown by the designation signal, and  
10 supplies the internal power to the circuit block as the  
11 operating power.

1 22. The nonvolatile memory microcomputer chip of Claim  
2 20,

3 wherein the nonvolatile memory includes a power  
4 circuit which serves as the power supply unit,

5 wherein the power circuit includes:

6 a step-up circuit operable to step-up the voltage  
7 of the external power; and

8 a voltage adjustment circuit operable to generate  
9 the internal power by stepping-down the stepped-up voltage  
10 of the external power to the voltage designated according

11 to the designation signal, and supply the internal power  
12 to the circuit block as the operating power.

1 23. The nonvolatile memory microcomputer chip of Claim  
2 1,

3 wherein the memory control unit (a) acquires a  
4 plurality of pieces of designation data from outside the  
5 nonvolatile memory microcomputer chip in a one-to-one  
6 correspondence with the plurality of pieces of test data,  
7 and stores each piece of test data and a corresponding  
8 piece of designation data in a memory area of the nonvolatile  
9 memory having a unique address, each piece of designation  
10 data being used for designating a current, and then (b)  
11 each time an address signal is given from outside the  
12 nonvolatile memory microcomputer chip, controls the  
13 nonvolatile memory to output a test signal and a designation  
14 signal which respectively show a piece of test data and  
15 a piece of designation data stored in a memory area having  
16 an address shown by the address signal,

17 the nonvolatile memory microcomputer chip further  
18 comprises:

19 a current judgment unit operable to judge whether  
20 a power supply current applied to the microcomputer unit  
21 exceeds a current designated according to the designation  
22 signal, and output a current judgment signal showing a

23 result of the judgment, and  
24 the output unit receives the current judgment signal  
25 from the current judgment unit, and outputs the current  
26 judgment signal to outside the nonvolatile memory  
27 microcomputer chip together with a test result signal  
28 received from a circuit block which is driven by the test  
29 signal.

1 24. The nonvolatile memory microcomputer chip of Claim  
2 23,

3 wherein the nonvolatile memory includes:  
4 a sense amplifier through which the power supply  
5 current passes, and which serves as the current judgment  
6 unit,

7 wherein the sense amplifier generates a reference  
8 current according to the designation signal, and outputs  
9 the current judgment signal based on a comparison between  
10 the reference current and the power supply current.

1 25. The nonvolatile memory microcomputer chip of Claim  
2 3,

3 wherein when a defective signal is given from outside  
4 the nonvolatile memory microcomputer chip in response to  
5 the test result signal and the expectation signal, the  
6 memory control unit stores the address shown by the address

7 signal to a predetermined memory area of the nonvolatile  
8 memory, the defective signal indicating that the circuit  
9 block is judged as being defective as a result of testing.

1 26. The nonvolatile memory microcomputer chip of Claim  
2 25,

3 wherein the memory control unit (a) acquires a  
4 plurality of instructions which constitute a program that  
5 is executable by the CPU, from outside the nonvolatile  
6 memory microcomputer chip, and stores each instruction  
7 in a memory area of the nonvolatile memory having a unique  
8 address, and then (b) when the defective signal is given  
9 from outside the nonvolatile memory microcomputer chip,  
10 stores the address shown by the address signal to the  
11 predetermined memory area of the nonvolatile memory, and  
12 subsequently supplies a control signal to the CPU, the  
13 control signal instructing to execute the program from  
14 an address of a memory area storing a beginning instruction.

1 27. The nonvolatile memory microcomputer chip of Claim  
2 4,

3 wherein the memory control unit supplies a data signal  
4 showing a non-operation instruction, to the CPU, and  
5 the CPU executes the non-operation instruction shown  
6 by the data signal a plurality of times to sequentially

7 output address signals which show consecutive addresses,  
8 thereby serving as the address generation unit.

1 28. A method for testing a nonvolatile memory microcomputer  
2 chip including a microcomputer unit and a nonvolatile  
3 memory unit, comprising:

4 a first test step of storing first test data in the  
5 nonvolatile memory unit, and then testing the microcomputer  
6 unit using the first test data in the nonvolatile memory  
7 unit to judge whether the microcomputer unit is defective;  
8 and

9 a second test step of storing, if the microcomputer  
10 unit is judged as being defective in the first test step,  
11 replacing the first test data in the nonvolatile memory  
12 unit with second test data, and then testing the  
13 microcomputer unit using the second test data in the  
14 nonvolatile memory unit.

1 29. A method for testing a plurality of nonvolatile memory  
2 microcomputer chips which each include a microcomputer  
3 unit and a nonvolatile memory unit, comprising:

4 a first test step of selecting a part of the plurality  
5 of nonvolatile memory microcomputer chips as test samples,  
6 storing first test data for performing testing about at  
7 least one test item in a nonvolatile memory unit of each

8 test sample, and then testing a microcomputer unit of each  
9 test sample using the first test data stored in the  
10 nonvolatile memory unit for each test item;  
11 a decision step of deciding, for each test item,  
12 whether all of the plurality of nonvolatile memory  
13 microcomputer chips need to be tested, based on a result  
14 of the testing in the first test step; and  
15 a second test step of storing second test data for  
16 performing testing about each test item for which all of  
17 the plurality of nonvolatile memory microcomputer chips  
18 are decided as needing to be tested, to a nonvolatile memory  
19 unit of each of the plurality of nonvolatile memory  
20 microcomputer chips, and then testing a microcomputer unit  
21 of each of the plurality of nonvolatile memory  
22 microcomputer chips using the second test data stored in  
23 the nonvolatile memory unit.

1 30. A method for testing a first nonvolatile memory  
2 microcomputer chip and a second nonvolatile memory  
3 microcomputer chip which each include a microcomputer unit  
4 and a nonvolatile memory unit, where the first and second  
5 nonvolatile memory microcomputer chips are connected so  
6 that data stored in a nonvolatile memory unit of the second  
7 nonvolatile memory microcomputer chip can be supplied to  
8 a microcomputer unit of the first nonvolatile memory

9 microcomputer chip, comprising:

10 a storage step of storing first test data for

11 performing testing about a first test item in a nonvolatile

12 memory unit of the first nonvolatile memory microcomputer

13 chip, and storing second test data for performing testing

14 about a second test item in the nonvolatile memory unit

15 of the second nonvolatile memory microcomputer chip;

16 a first test step of testing the microcomputer unit

17 of the first nonvolatile memory microcomputer chip using

18 the first test data stored in the nonvolatile memory unit

19 of the first nonvolatile memory microcomputer chip;

20 a supply step of supplying the second test data stored

21 in the nonvolatile memory unit of the second nonvolatile

22 memory microcomputer chip, to the microcomputer unit of

23 the first nonvolatile memory microcomputer chip; and

24 a second test step of testing the microcomputer unit

25 of the first nonvolatile memory microcomputer chip using

26 the second test data supplied from the nonvolatile memory

27 unit of the second nonvolatile memory microcomputer chip.